R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 9 lines 6-15 and FIG. 2 and claims 1 and 11 as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 1 under 35 U.S.C. §112, second paragraph, is respectfully traversed and should be withdrawn.

The specification provides examples on page 4, lines 15-17 for the claimed "assembly apparatus." In particular, one of ordinary skill of the art for the present application would be aware that silicon die may be mounted to ceramic substrates, metal housings and plastic housings. Therefore, the specification does provide sufficient information such that one of ordinary skill in the art would reasonably understand the scope of the invention and thus the claim is definite. As such, claim 1 is fully complaint with 35 U.S.C. §112, second paragraph and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-19 under 35 U.S.C. §102(e) as being anticipated by Matsunami, et al. Publication No. U.S. 2003/0191910 (hereinafter Matsunami) is respectfully traversed and should be withdrawn.

Matsunami concerns a disc storage system including a switch (Title). In contrast, claim 1 provides (in part) an assembly apparatus mounting a programmable logic device (PLD) and a die. In contrast, Matsunami appears to be silent regarding an assembly apparatus mounting a PLD and another die. Furthermore, page 2, section 3 of the Office Action provides no evidence or arguments that Matsunami discloses the claimed assembly apparatus.

Claim 1 further provides a programmable logic device. The website www.webopedia.com provides a common definition for a programmable logic device as:

> A generic term for an integrated circuit that can be programmed in a laboratory to perform complex functions. A PLD consists of arrays of AND and OR gates. A system designer implements a logic design with a device programmer that blows fuses on the PLD to control gate operation.

Despite the assertion on pages 2-3, section 3 of the Office Action, the text of Matsunami in paragraphs [0069], [0008-0009] and [0043-0045] appears to be silent regarding a PLD. Therefore, Matsunami does not appear to disclose or suggest a PLD as presently claimed.

Claim 1 further provides a die comprising a first communication channel (i) configured to convert between a first serial data signal and a first parallel data signal and (ii) coupled to a first of a plurality of routing channels of the PLD to exchange the first parallel data signal with at least one of a plurality of logic block clusters of the PLD. In contrast, Matsunami appears to be silent regarding a die configured to convert between serial and parallel signals being coupled to a PLD to exchange the parallel signals with at least one logic block cluster of the PLD. Despite the assertion on page 3 of the Office Action, the software button 5002 within the console screen 50 in FIG. 18 of Matsunami does not appear to be a die. Likewise, a fibre channel protocol controller 20233 shown in FIG. 16 of Matsunami does not appear to be a die. No evidence has been provided and Matsunami appears to be silent regarding both the software button 5002 and the fibre channel protocol controller 20233 being configured to convert between serial and parallel signals. Furthermore, no evidence has been provided and Matsunami appears to be silent regarding the fibre channel protocol controller 20233 being coupled to a PLD to exchange parallel data signals with a logic block cluster in the PLD. Therefore, Matsunami does not appear to disclose or suggest a die comprising a first communication channel (i) configured to convert between a first serial data signal and a first parallel data signal and (ii)

coupled to a first of a plurality of routing channels of a PLD to exchange the first parallel data signal with at least one of a plurality of logic block clusters of the PLD as presently claimed. Claims 11 and 19 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 11 further provides steps for (a) mounting a programmable logic device, (b) mounting a die, and (c) coupling a first communication channel of the die to a first routing channel of the PLD. In contrast, Matsunami appears to be silent regarding a method for fabricating the disc storage system disclosed therein. Therefore, Matsunami does not appear to disclose or suggest the steps of (a) mounting a programmable logic device, (b) mounting a die, and (c) coupling a first communication channel of the die to a first routing channel of the PLD as presently claimed. Therefore, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides a die comprising a first communication channel (from claim 1) and a second communication channel. Similarly, claims 3 and 4 provide for a third communication channel and a fourth communication channel, respectively. Despite the assertion on page 3 of the Office Action, Matsunami appears to be silent regarding the fibre channel protocol controller 20233 having multiple communications channels. Therefore, Matsunami does not

appear to disclose or suggest a die comprising a first communication channel, a second communication channel, a third communication channel and a fourth communication channel as presently claimed. Claim 5 provides language similar to claim 2. Claims 12-15 provide language similar to claims 2-5. As such, claims 2-5 and 12-15 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a first communication channel coupled to a first routing channel to receive a control signal from one of a plurality of logic block clusters of a PLD. Despite the assertion on page 5 of the Office Action, Matsunami appears to be silent regarding each of (i) a PLD, (ii) a plurality of logic block clusters in the PLD, (iii) a control signal generated by one of the logic block clusters and (iv) the control signal being received by a first communication channel of a die. Therefore, Matsunami does not appear to disclose or suggest a first communication channel coupled to a first routing channel to receive a control signal from one of a plurality of logic block cluster of a PLD as presently claimed. Claim 16 provides language similar to claim 6. As such, claims 6 and 16 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 7 provides a control signal configured as one of (i) a portion of a first parallel signal and (ii) an encoding selection signal. In contrast, Matsunami appears to be silent

regarding a control signal as discussed above for claim 6. Therefore, Matsunami does not appear to disclose or suggest a control signal configured as one of (i) a portion of a first parallel signal and (ii) an encoding selection signal as presently claims. The Examiner is respectfully requested to either (1) provide clear and concise explanation how a frame header and a frame configuration of Matsunami imply a portion of a signal and an encoding selection signal or (2) withdraw the rejection.

Claim 10 provides a die comprising a first communication channel and a second communication channel. In contrast, Matsunami appears to be silent regarding a die having multiple communication channels. Furthermore, page 5 of the Office Action offers no evidence or arguments regarding claim 10. Therefore, Matsunami does not appear disclose or suggest a die comprising a first communication channel and a second communication channel as presently claimed. The Examiner is respectfully requested to provide either (1) a clear and concise explanation how Matsunami anticipates the claim limitations or (2) withdraw the rejection.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a non-final action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No arguments or evidence was directed to claim 10. Furthermore, the Examiner is respectfully requested to avoid omnibus rejections that merely cite large sections of text and assert that the claim elements are somehow anticipated (see MPEP 707.07(d)). As such, the Office Action mailed December 8, 2003 was not complete.

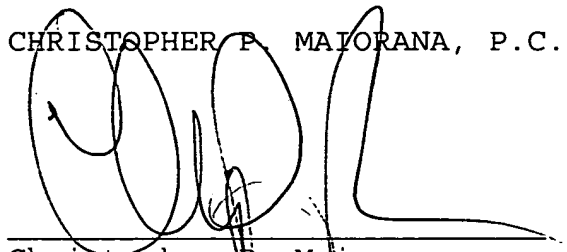
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: March 8, 2004

Docket No.: 0325.0485